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EATON, K	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

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Office Action Summary	Application No. 09/599,783	Appli ant(s) FURUKAWA ET AL.	
	Examiner Kurt M. Eaton	Art Unit 2823	

-- The MAILING DATE of this communication app ars on th cover sheet with the correspond nce address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2000* is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the etching of the semiconductor substrate, the forming of the doped regions in the semiconductor substrate, and the forming of the dielectric and conductive structures over the semiconductor substrate must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cho et al. in view of Juengling.

In re claims 1, 9, and 15, Cho et al. (herein referred to as Cho) shows, in an analogous art related to a method for fabricating a semiconductor device, in Figures 3-8 forming a dielectric layer stack (32/34/36) over a major surface of a semiconductor substrate (30); forming a patterning mask (31); selectively etching the dielectric layer through the patterning mask to form an opening (39) in the dielectric layer; and selectively etching the semiconductor substrate through the opening in the dielectric layer {column 1, line 10 - column 4, line 35}.

Cho does not show wherein the step of forming the patterning mask includes depositing a layer of metallic germanium over the dielectric layer and patterning the layer of metallic germanium to form a germanium hard mask.

Juengling shows, in an analogous art related to the manufacture of semiconductor devices, in Figures 1, 3, and 4 forming a dielectric layer (12/14) over a major surface of a semiconductor substrate (10); depositing a layer of metallic germanium (16) over the dielectric layer; patterning the layer of metallic germanium to form a germanium hard mask; and selectively etching the dielectric layer through the germanium hard mask. Juengling teaches wherein metallic germanium may be used as an effective anti reflective coating for use in photolithographic procedures which enhances line width control, reduces feature tolerances, and allows for more aggressive circuit design. Metallic germanium also facilitates the complete removal of photoresists {column 1, line 24 - column 4, line 33}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the patterning mask of Cho to include a deposited germanium hard mask as found in Juengling over the dielectric layer of Cho prior to the step of forming the opening in the dielectric layer of Cho since the provision of the germanium hard mask over the dielectric layer would enhance the controllability of the process, reduce feature tolerances, and allow for an aggressively designed circuit.

In re claims 2, 10, and 18, Cho shows wherein the step of forming the patterning mask includes forming and patterning a layer of photoresist material (31). Cho further includes a step of removing the layer of photoresist material after performing the step of selectively etching the dielectric layer, wherein the layer of photoresist material is stripped {column 4, lines 9-35}.

Cho does not further include a step of stripping away a layer of metallic germanium after performing the step of selectively etching the dielectric layer.

Juengling shows wherein the germanium hard mask is formed according to a method including steps of depositing a layer of photoresist over the layer of metallic germanium and patterning the layer of metallic germanium to form the germanium hard mask. Juengling further includes a step of stripping the layer of photoresist material and the layer of metallic germanium after performing the step of selectively etching the dielectric layer, wherein the layer of photoresist and the layer of metallic germanium are stripped using an ashing/strip process {column 3, line 60 - column 4, line 18}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the ashing/strip process of Juengling in the step of removing the layer of photoresist material in the invention of Cho in view of Juengling since Cho is silent as to the specific removal process used and the ashing/strip process of Juengling would enable one of ordinary skill in the art to remove the layer of photoresist material of Cho found in the invention of Cho in view of Juengling. It also would have been obvious that the layer of metallic germanium of Cho in view of Juengling also would have been stripped upon carrying out the ashing/strip process of Cho in view of Juengling since the metallic germanium layer of Juengling is stripped upon application of the ashing/strip process of Juengling.

In re claims 3, 11, and 19, Juengling shows wherein the step of stripping away the layer of metallic germanium includes the steps of oxidizing the layer of metallic germanium to form a layer of germanium oxide therefrom; and removing the layer of germanium oxide {column 3, line 60 - column 4, line 18}.

In re claims 4, 11, and 20, Juengling shows wherein the step of removing the layer of germanium oxide includes rinsing the semiconductor substrate in a "piranha" cleaning solution {column 3, line 60 - column 4, line 18}.

Cho in view of Juengling does not show wherein the step of removing the layer of germanium oxide includes rinsing the semiconductor substrate in water.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that, upon rinsing the semiconductor substrate of Cho in view of Juengling in a "piranha" cleaning solution, the semiconductor substrate would have been rinsed in water since it is well known in the art that a "piranha" cleaning solution includes H_2SO_4 and H_2O_2. It is also well known that upon its application, the H_2O_2 of which the "piranha" cleaning solution includes, decomposes into water. Accordingly, it would have been obvious to one of ordinary skill in the art that the step of removing the layer of germanium oxide would have included rinsing the semiconductor substrate in water.

In re claim 5, Cho in view of Juengling shows wherein the step of stripping away the layer of metallic germanium includes stripping away the layer of metallic germanium before performing the step of selectively etching the semiconductor substrate.

In re claims 6, 12, and 16, Juengling shows wherein the step of depositing the layer of metallic germanium includes depositing the layer of metallic germanium to a thickness between approximately 40 nm and approximately 500 nm {column 3, lines 45-46}.

In re claims 7, 13, 16, and 17, Juengling shows wherein the patterning the layer of metallic germanium to form the germanium hard mask includes the steps of depositing a layer of photoresist over the layer of metallic germanium; exposing and developing the photoresist layer to form a

photolithography image ; and patterning by etching the layer of metallic germanium through the photolithography image to form the germanium hard mask. {column 3, line 60 - column 4, line 18}.

In rc claims 8 and 14, Cho shows wherein the step of forming the dielectric layer further includes the steps of forming a pad oxide layer (32) over the major surface of the semiconductor substrate; depositing a nitride layer (34) over the pad oxide layer; and forming a mask oxide layer (36) over the nitride layer, wherein the mask oxide layer is formed by a high temperature oxidation process {column 3, line 61 - column 4, line 35}.

Cho in view of Juengling fails to show wherein the step of forming the pad oxide layer to a thickness between approximately 5 nm and approximately 30 nm; depositing the nitride layer to a thickness between 50 nm and approximately 300 nm over the pad oxide layer; and depositing the mask oxide layer to a thickness between 800 nm and approximately 3,000 nm over the nitride layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the mask oxide layer of Cho in view of Juengling through a deposition process since deposition processes used to form oxide layers are well known in the art and the selection of a known oxide formation process on the basis of its suitability for its intended use involves only routine skill in the art. Furthermore, the specification contains no disclosure of either the critical nature of the claimed mask oxide formation process or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen oxide formation processes or upon another variable recited in a claim, the applicant must show that the particular oxide formation processes are critical. It also would have been obvious to form the pad oxide, nitride, and mask oxide layers within the dielectric layer of Cho in view of Juengling to thicknesses between approximately 5 nm and approximately 30 nm, between 50 nm and approximately 300 nm, and between 800 nm and approximately 3,000 nm, respectively, since thicknesses of individual layers within a multilayered

dielectric layer are well known processing variables and the discovery of the optimum or workable ranges involves only routine skill in the art. Furthermore, the specification contains no disclosure of either the critical nature of the claimed thickness ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensional ranges or upon another variable recited in a claim, the applicant must show that the particular dimensional ranges are critical.

In re claim 9, the invention of Cho further relates the method disclosed therein towards the use of trenches used to isolate devices in CMOS and bipolar circuits {column 1, lines 10-41}.

Cho in view of Juengling fails to show forming doped regions in the semiconductor substrate and forming dielectric and conductive structures over the semiconductor substrate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that practitioners of Cho in view of Juengling would have formed doped regions in and dielectric/conductive structures over the semiconductor substrate of Cho in view of Juengling since the formation of doped regions in and dielectric/conductive structures over semiconductor substrates used in CMOS and bipolar circuits is well known in the art and, while Cho is primarily concerned with trench formation, the method of Cho is related to a method used in CMOS and bipolar circuit formation.

In re claim 12, Juengling shows depositing the metallic germanium layer in a CVD process {column 3, lines 45-47}.

Conclusion

4. Paper related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in

the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication of earlier communication from the examiner should be directed to **Kurt Eaton** at **(703) 305-0383** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via kurt.eaton@uspto.gov.

SUPERVISORY PRIMARY EXAMINER
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